REMARKS/ARGUMENTS

Regarding amendments to the specification:

The specification is amended to overcome the objections set forth on the following detailed Office action, emphasize the characteristics of the claimed invention, and in the interests of clarity is reproduced above in toto. (Amendments are indicated in the standard way and the original page/line formatting has been retained as far as practicably possible.)

Other minor grammatical and otherwise objectionable errors have been corrected where detected. No new matter is entered by the above amendments.

Regarding amendments to the claims:

Claims 1-12 are amended to overcome the objections set forth on the following detailed Office action, emphasize the characteristics of the claimed invention, and in the interests of clarity is reproduced above in toto. Claims 13-16 are added to further highlight the application of the claimed invention, such that the package structure described in the claim 14 (a connection between the semiconductor chip and the leading wires) has been widely taught in numerous related arts. Hence, no new matter is entered by the above amendments.

Regarding rejections under 35 U.S.C. 102 and 35 U.S.C. 103:
Examiner:

1. **Claims 1 and 3-6 are rejected under 35 U.S.C 102(b) as being anticipated by Terui et al (US Pat. 6608375).**

Referring to claim 1, Terui et al. discloses a package structure comprising: a lead frame (Fig. 36 and 37A-B #1722), having a plurality of first leads (#1711), each of which includes a first recession (area of #1711); at least a first device (#1710); and a plurality of solder joints (#1712), respectively positioned in the first recessions (area of #1711), for connecting the first device (#1710), to the lead frame (#1722).

Response:

According to Fig. 36 and 37A-B of Terui et al, a conductive wiring pattern (1722) is formed over the surface of an organic substrate (1721), in which the organic substrate (1721) further includes a plurality of cavities (1727). Additionally, each of the cavities (1727) is provided with a chip capacitor mounting pad (1711), and a plurality of chip capacitors (1710) are mounted on the chip capacitor mounting pads (1711) in the cavities (1727) with a conductive adhesive (1712).

Claims 1, and 3-6 are amended to overcome this rejection, in which the claims 5 and 6 are cancelled. According to the amended claim 1, the claimed invention teaches a packaging structure comprising a lead frame having a plurality of first leads, in which each of the first leads includes a first recession, and a plurality of solder joints respectively positioned in the first recessions to connect a semiconductor chip to the lead frame. Essentially, each lead of the claimed invention includes a recession respectively. In other words, the recession is formed within the lead, such that the solder joints and the recession combination functions to support the semiconductor chip and prevent the chip from any movement during reflow processes. However, the lead taught by Terui et al, represented by the capacitor mounting pad (1711), is disposed over the surface of the recession, represented by the area of the capacitor mounting pad (1711). The semiconductor chip taught by Terui et al on the other hand, is directly mounted over the surface of a die pad and suggests no means of support from the combination of the recession and the solder joints. Hence, the packaging structure of the claimed invention is significantly different from the one taught by Terui et al.

According to Chapter 2112 in the MPEP, in relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art. Since the inherency of a lead frame package structure does not flow from the teachings of Terui et al, the amended claims 1,3 and 4 should be novel based on the above analysis, and since the amended claims 3 and 4 are dependent upon claim 1, the amended claims 3and 4 should be allowed if claim 1 is allowed. Reconsideration of the amended claims 1,3 and-4 is politely requested.

2. Claim 7 is rejected under U.S.C 103(a) as being unpatentable over U.S. Pat. 6608375 Terui et al. in view of U.S. Patent No. 6127206 Nakamichi.

Response:

Claim 7 is cancelled and added to the amended claim 2. The semiconductor chip taught by Terui et al is directly mounted over the surface of a die pad, and suggests no means of support from the combination of the recession and the solder joints. Additionally, Terui et al never suggests a lead frame having a plurality of second leads and each lead includes a second recession. Despite the fact that Nakamichi teaches a recession (groove 18) on the lead (16), the semiconductor chip (20) is loosely connected to the leads via wire boding, and suggests no means of support from the combination of the recession and solder joints as in the claimed invention.

Since the package structures taught by Nakamichi and Terui et al are significantly different from the one taught by the claimed invention, those skilled in the art would find it physically impossible to combine the references in the manner suggested.

3. Claims 8 and 9 are rejected under U.S.C 103(a) as being unpatentable over U.S. Pat. 6608375 Terui et al. in view of U.S. Patent No. 6127206 Nakamichi in further view of U.S. Patent No. 5682057 Kuriyama.

Response:

According to Fig. 1-4 of Nakamichi et al, a semiconductor chip 20 is mounted on the island 12 of the lead frame 1 with an adhesive. An electrode pad 22 of the semiconductor chip 20 is bonded to the inner lead 16a of the lead 16 with the wire 24, and the wire 24 is bonded inside the groove18 of the inner lead 16a.

Claims 8 and 9 are amended and claims 13-16 are added to overcome this rejection, in which claim 8 is cancelled and added to the amended claim 3. According to the added claims, a package structure comprising a lead frame having a plurality of first leads, in which each of the first leads includes a first recession, at least a passive device, in which each output of the passive device is respectively positioned in the first recessions, and a plurality of first solder joints respectively positioned in the first recessions for connecting the passive device to the lead frame. Preferably, the limitation of the first recessions

prevents the passive devices from movement. Additionally, the package structure also includes a semiconductor chip, in which the semiconductor chip can be connected to a plurality of leading wires or connected to the lead frame by positioning a plurality of second solder joints in the second recessions of a plurality of second leads. Despite the fact that Nakamichi teaches the chip bonded to the lead with the wire, and the wire is bonded inside the groove of the lead, the semiconductor chip (20) is loosely connected to the leads via wire boding, and suggests no means of support from the recession (first groove 18) as in the claimed invention. On the other hand, the recessions taught by Terui et al are provided with two leads (represented by the capacitor mounting pad (1711), and the pad at the bottom of cavities (1727) the connected to the die pad (1701)), such that the chip capacitor (1710) is mounted in a recession, and suggests no means of support from the outputs of passive device respectively positioning in a recession of each lead. Moreover, the combination of wire bonding and connection of a device by situating solder joints within the recessions of a plurality of leads has already been suggested by the added claims, in which the technique of wire bonding has been widely taught in numerous related arts.

Since the package structures taught by Nakamichi and Terui and Kuriyama et al are significantly different from the one taught by the claimed invention, those skilled in the art would find it physically impossible to combine the references in the manner suggested. Moreover, since claim 9 is dependent upon the amended claim 3, claim 9 should be allowed if the amended claim 3 is allowed. Reconsideration of amended claims 3 and 9 is politely requested.

4. Claims 1, 2 and 10-12 are rejected under U.S.C 103(a) as being unpatentable over U.S. Patent No. 6127206 Nakamichi in view of U.S. Patent No. 5682057 Kuriyama.

Response:

Claims 1, 2, 10-12 are amended to overcome this rejection, in which the original claim 2 has been combined with claim 1. Despite the fact that Nakamichi teaches the chip bonded to the lead with the wire (solder joints), and the wire is bonded inside the recession (first groove 18) of the lead, the wire and the recession combination are

nevertheless unable to support the chip (20). In other words, the semiconductor chip (20) is loosely connected to the leads via wire boding, and suggests no means of support from the solder joints and recession as in the claimed invention.

Despite the fact that Kuriyama teaches that the conductor strip can be composed of solder, the semiconductor chip is directly mounted over the surface of a base plate, and suggests no means of support from solder joints and recessions. Hence, Kuriyama never suggests a packaging structure with a lead frame having a plurality of first leads and each lead includes a first recession, and a plurality of solder joints positioned in the first recession for connecting a semiconductor chip to the lead frame. Therefore, provided that the semiconductor device taught by Kuriyama and the package structure taught by Nakamichi are significantly different than the claimed invention, those skilled in the art would find it physically impossible to combine the two references in the manner suggested. Moreover, the amended claims 10, 11, and 12 are dependent upon claim 1, hence the amended claims 10, 11, and 12 should be allowed if claim 1 is allowed. Reconsideration of claims 1and 10-12 is politely requested.

In view of the above arguments in favor of patentability, the applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

Winston Hsu Date: November 18, 2005

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)